FEASIBILITY STUDY OF SILICON PIXEL DETECTOR

By

Tris Tanadi
tristan@iastate.edu

Table of Contents

1. Motivation of using silicon pixel detector

A monolithic active pixel sensor for charged particle tracking based on a novel detector structure is adapted from IreS/Lepsi work [1]. The idea is for detecting element and the readout electronics are integrated onto the same low-resistivity silicon wafer. There are couple advantages of this monolithic pixel sensor idea [1],

- Thin device → reduced the effect of multiple scattering
- No detector-electronic connection

The idea of monolithic pixel sensor can be done with a CMOS fabrication process. CMOS process is basically chose because of some of the factors below:

- Well-established fabrication process
- Lower power usage
- Lower system cost
- The flexibility of integrating additional circuitry on chip
- High yield
- Convenient way of design

2. Diode Structure

The idea and basic architecture for the detector/diode is adopted from digital still and video cameras. In silicon pixel detector, the diode needs to collect the electrons that generated from the particle hit. The cross section of the diode can be seen on figure 1.

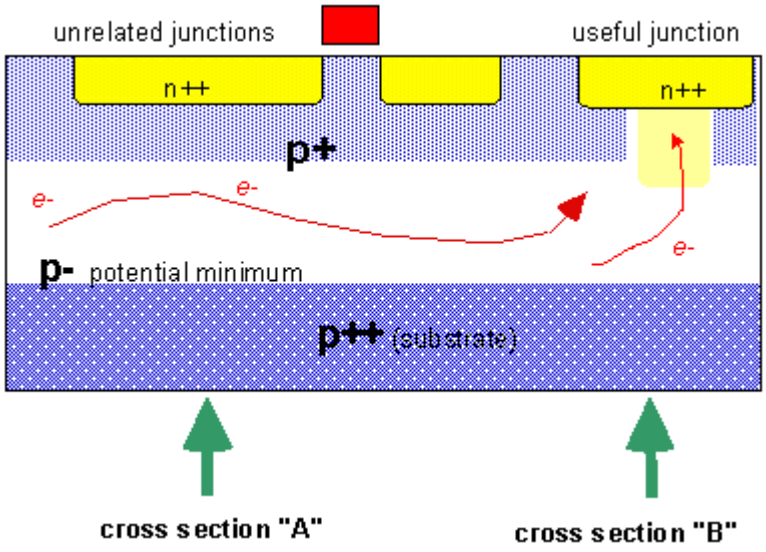

Figure 1. Cross section of the diode structure [2]

The above device can be fabricated using a standard CMOS process. This approach will allow the diode to detect the electrons generated in the epi-layer beneath the surface of the whole pixel (electrons that are normally lost); this will effectively increase the fill factor.

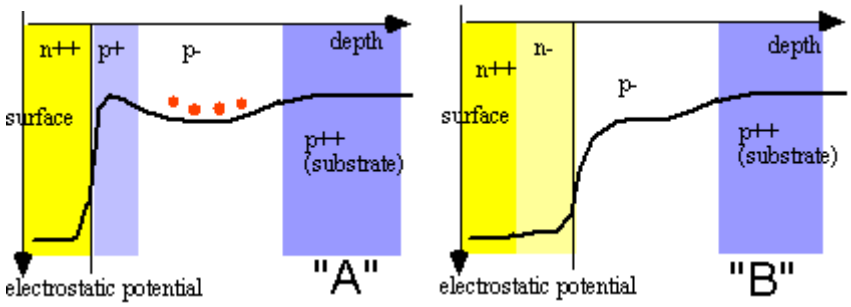

Figure 2. Electrostatic Potential across the diode [2]

We are in the process of simulating the diode to see how it will able to collect all of the electrons that generated by the particle hit. Schematically in cross section "A" of figure 2, we can clearly see how all the electrons generated in the p- area (epi-layer) diffuse to the cross section "B" where they are collected in the n-well.

3. Technical Challenges

The main challenge of this detector is to make sure that the detector can detect all or most events that happen in the collider. MIMOSA chips that developed by IReS/LEPSI are using the serial readout. We can decrease the total time to read out all of the information from the array by having a column parallel readout.

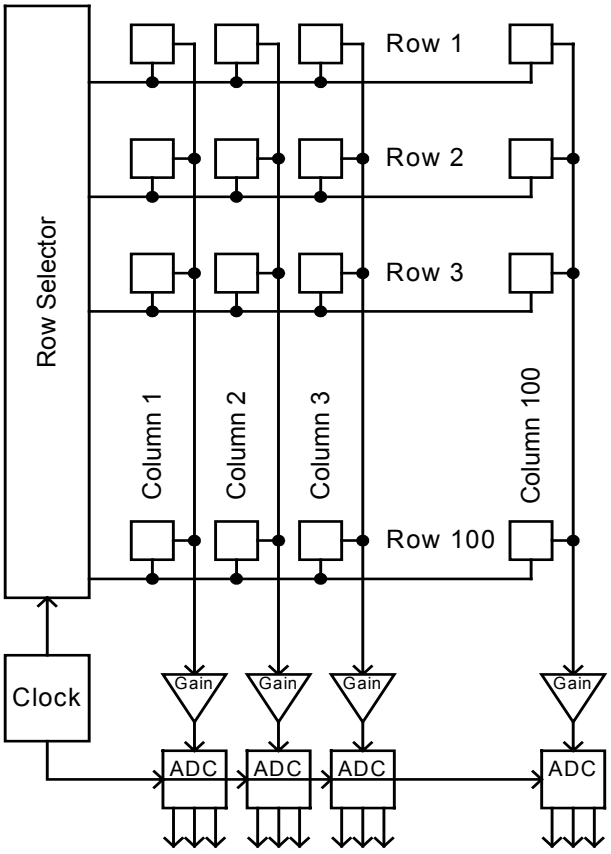

Figure 3. Schematic Block Diagram

There are a lot of pixels in each array, so we have to make sure that all pixels are going to have a similar characteristic. The noises affect each pixel has to be low or be uniform so we can calibrate or subtract the noise at the end.

In order to make sure the column in parallel readout to work, a sampling and hold functionality has to be performed on each pixel. This sampling and hold is necessary because pixels on different row have to wait for the pixels on the previous row to be readout. It is also important to insure this waiting period will hold the integrity of the signal that is hold on each pixel.

Doing the readout in column in parallel will increase the number of the gain and analog-to-digital circuit by the number of columns in the array. Power consumption will become a big issue in this case. Reasonable power consumption for the whole chip is required.

Even though doing the read out in this fashion will reduce the readout time significantly, we still have to make sure that readout time for the whole pixels will be smaller than the time for the next possible collisions or Level-1 Trigger.

Currently there is no pipelining employed in the design but it is something that we need to look at to improve this design so any suggestions on how to employ the pipelining would be warmly welcomed.

4. Pixel Structure

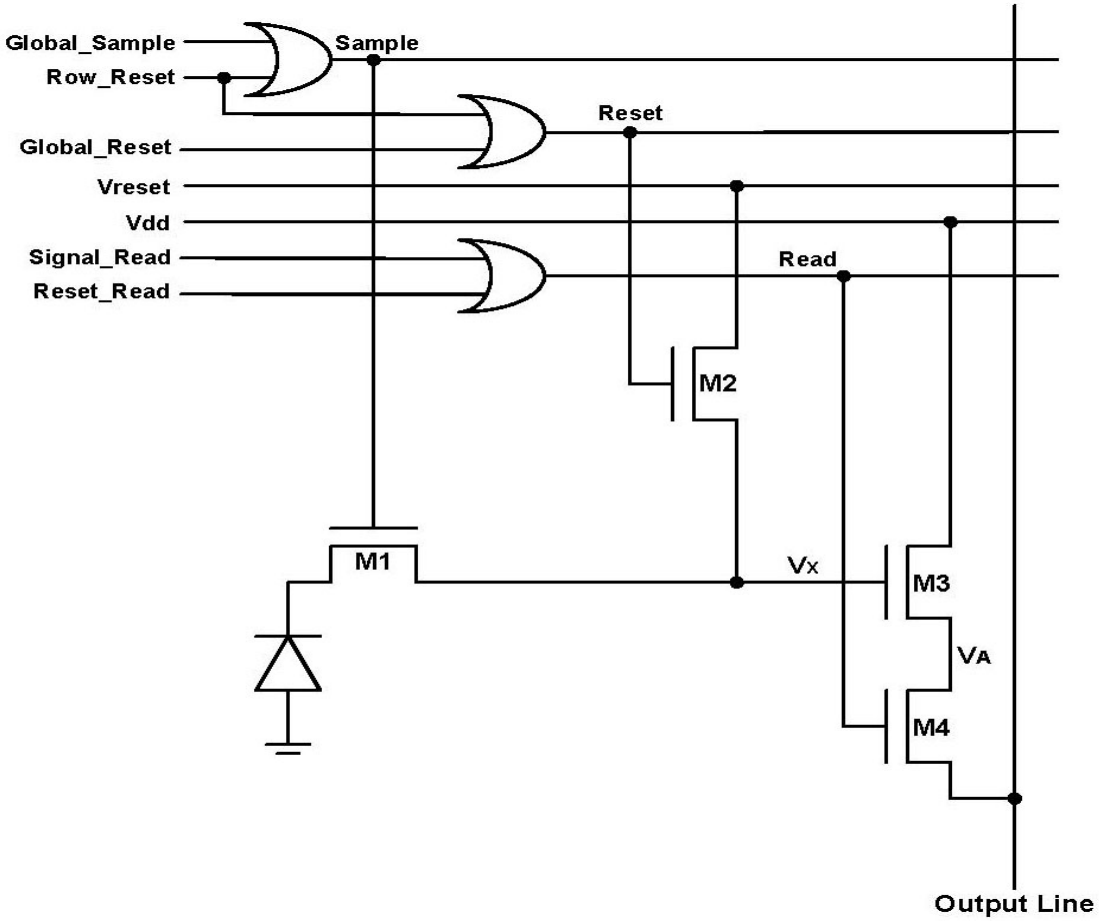

Figure 4. Proposed Pixel Structure

The schematic level of the proposed pixel structure can be seen on figure 4. This structure will be improved in the next few pages. Each individual pixel is comprised of only 4 MOS transistors and a diode to collect the charge. The logic gates (OR gates) are only shown for clarity purposes and they are not actually inside the pixel. All of the logic gates will be implemented in the row selection.

This pixel structure is adapted from the IreS/Lepsi [1]. The structure from MIMOSA I and MIMOSA II is only consist of 3 n-channel transistors. In our proposed design, we have an extra transistor (M1 on Figure 4) to perform the sample and hold function on the pixel.

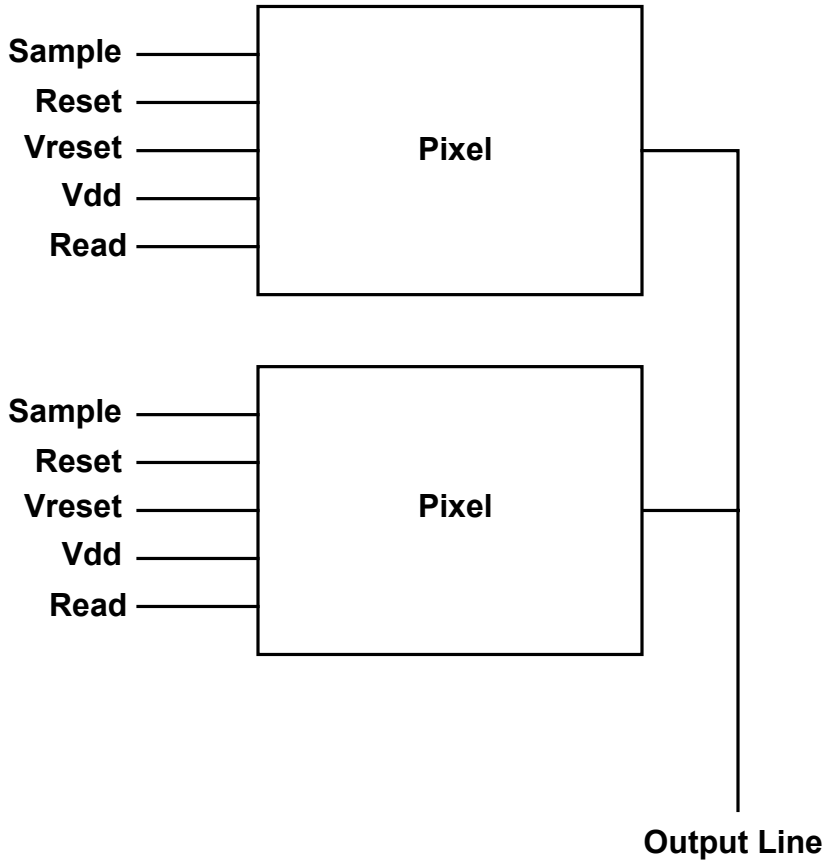

Figure 5. The Actual Pixel Symbol

The symbol of two pixels is shown in figure 5. There are only five signals that coming in to each pixel instead of 7 signals shown on figure 1. All of the pixels in the same column will share the same output line.

4.1. Signal Definition and Sequences

There are 10 signals from figure 1 that we are interested in. Those signals plus a brief definition are as follow:

- Global_Reset: To reset all pixels on the chip.
- Row_Reset: To reset all pixels on a particular row.
- Reset: The “OR” logic value between Global_Reset and Row_Reset.
- Signal_Read: To read the sampling signal.
- Reset_Read: To read the reset signal.
- Read: The “OR” logic value between Signal_Read and Reset_Read.
- Global_Sample: To provide the sampling time for all pixels on the chip.
- Sample: The “OR” logic value between Global_Sample and Row_Reset.

All the above signals are integrated as a sequence and the signals are changing appropriately with certain timing and trigger signals. The sequence on one row of the array is shown in timing diagram on the next couple pages.

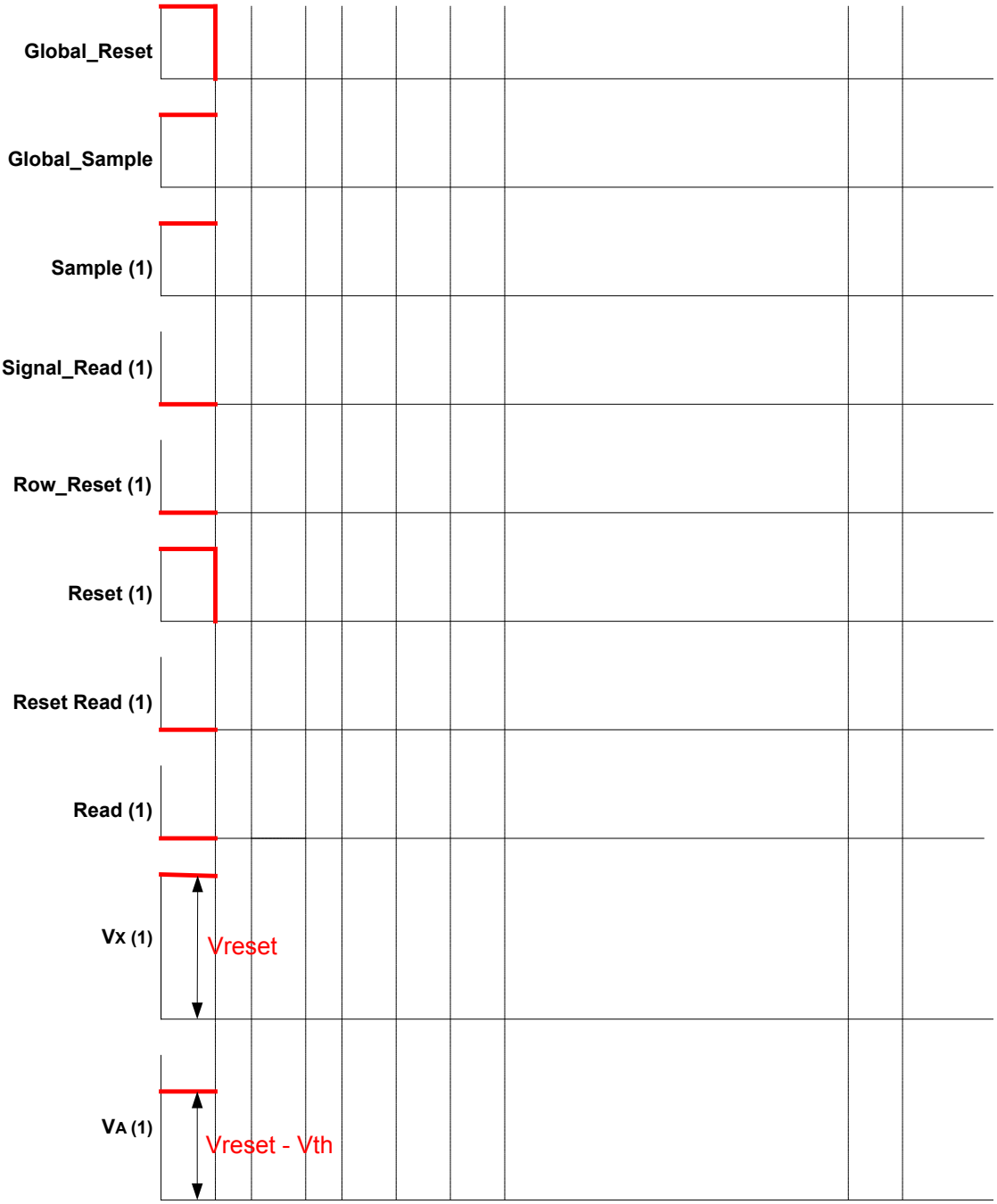

Figure 6. Sequence 1

Global_Reset and Sample go high at the same time. This will charge Vx to Vreset. And the same time we reset the diode by forcing the diode to a known voltage reset.

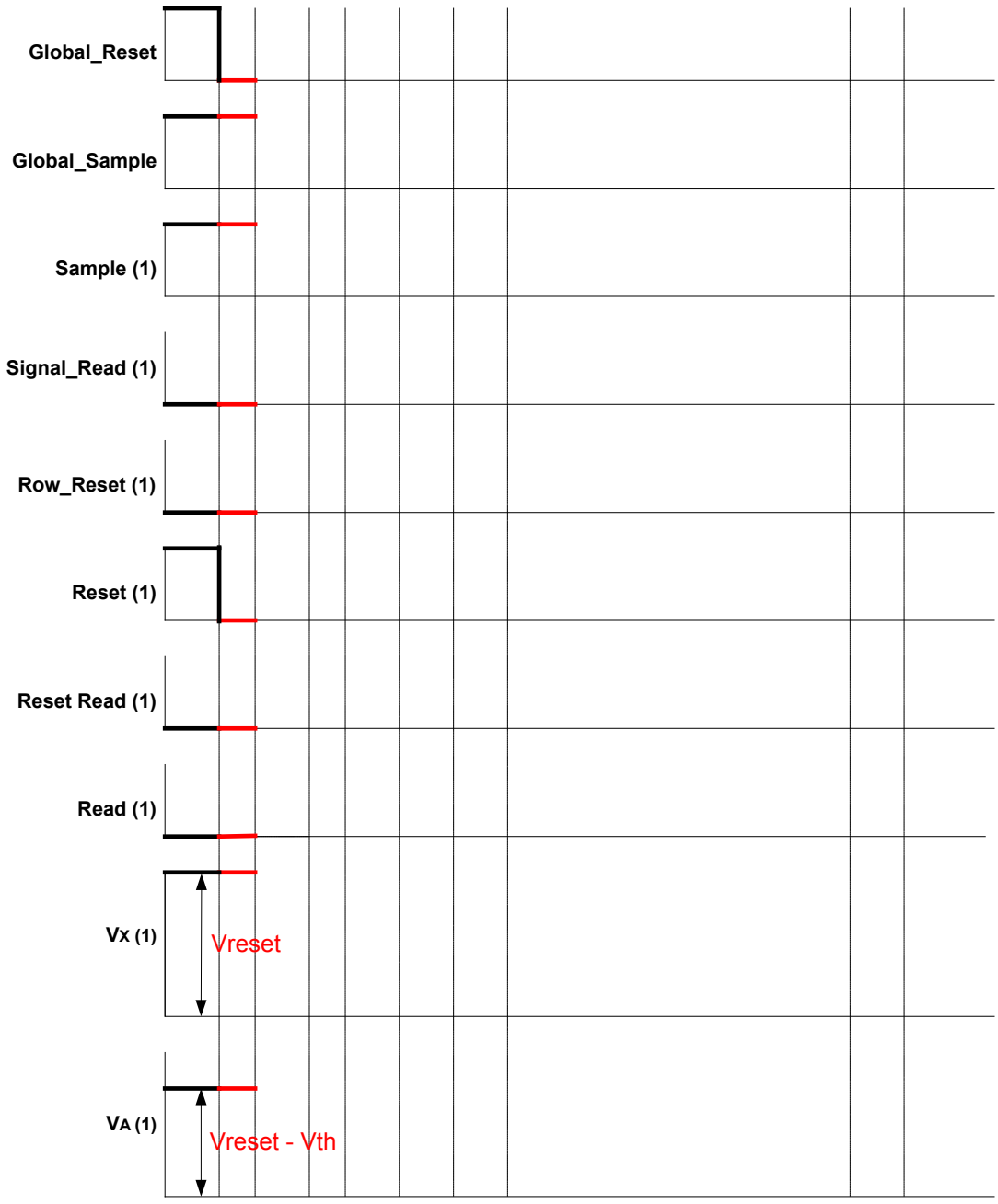

Figure 7. Sequence 2

Global_Reset goes low and Sample stays high mean the pixel is in the sampling mode. The pixel is ready for any particles hit. In this state, the pixel is waiting for a collision and particle hit.

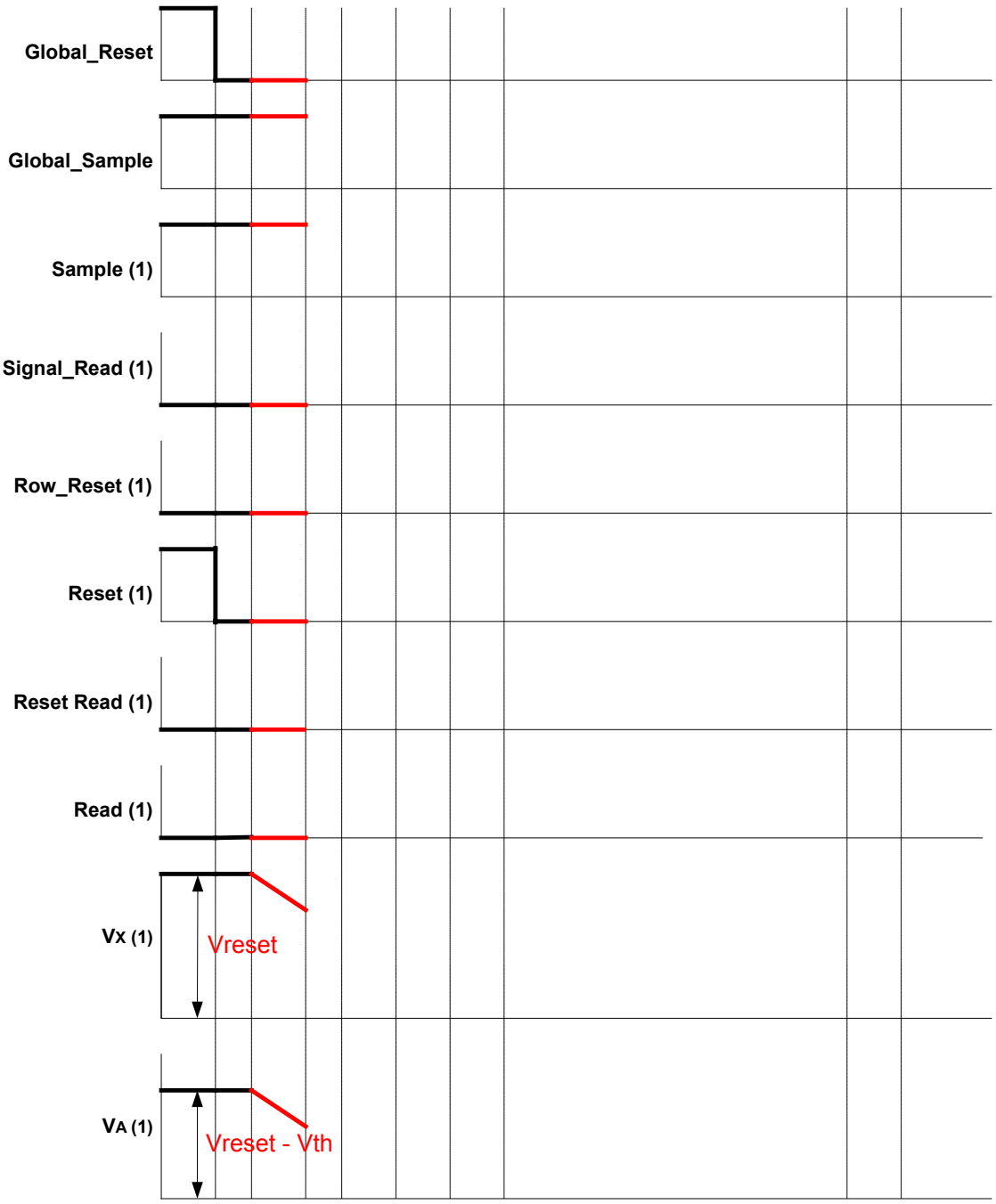

Figure 8. Sequence 3

Sample remains high and there are particles hit on the pixel and charges are collected by diode. Vx and Va voltages are being discharged by the hit.

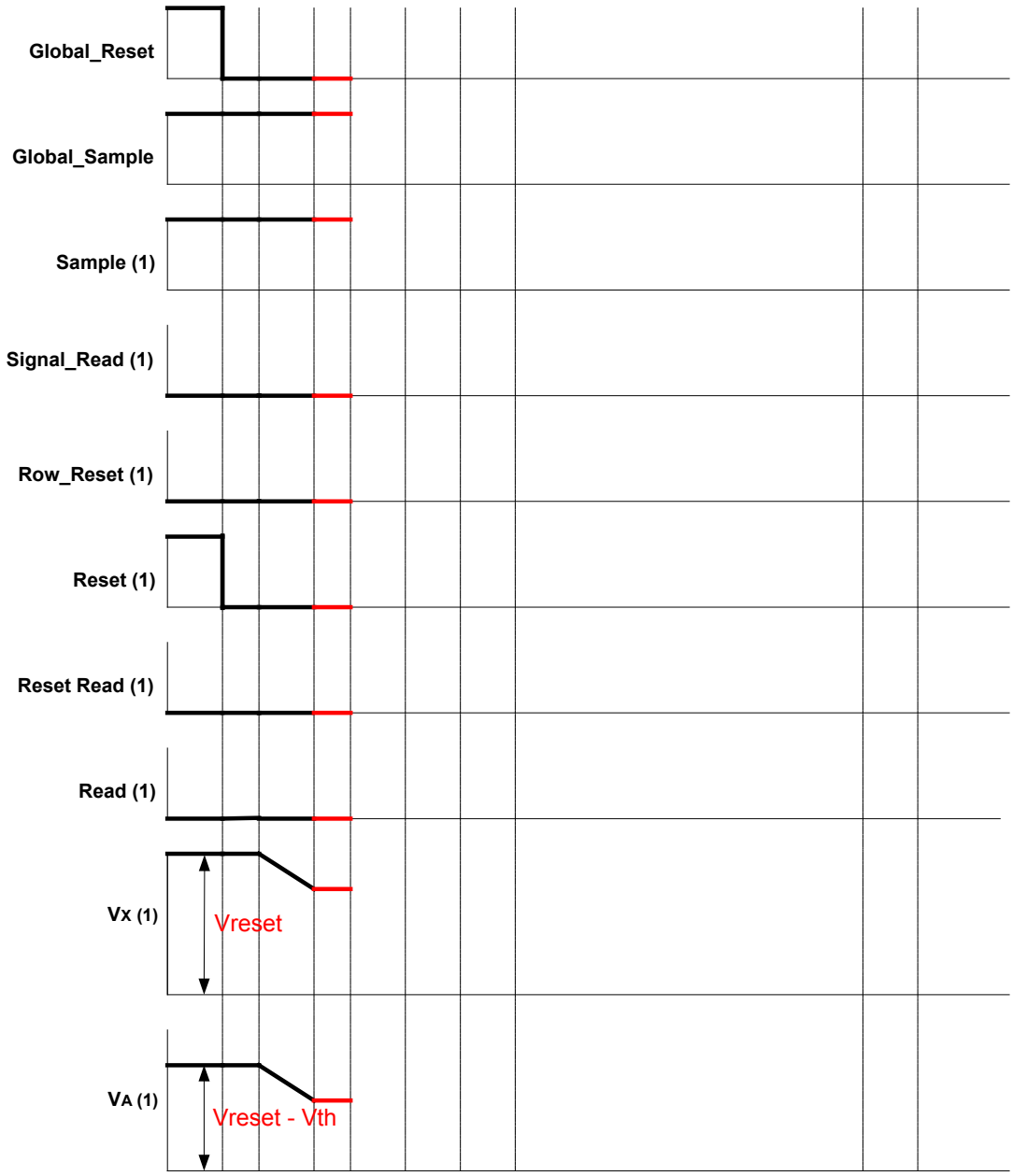

Figure 9. Sequence 4

Sample is still high but there is no more particles hit. This sampling period can be stopped by a trigger from Level 1 signal or we can do it with a fixed time period. The signal collected is cumulative of many beam crossings until the trigger is received or the sampling time is up. Because there is no pipelining the pileup events will need to be rejected offline.

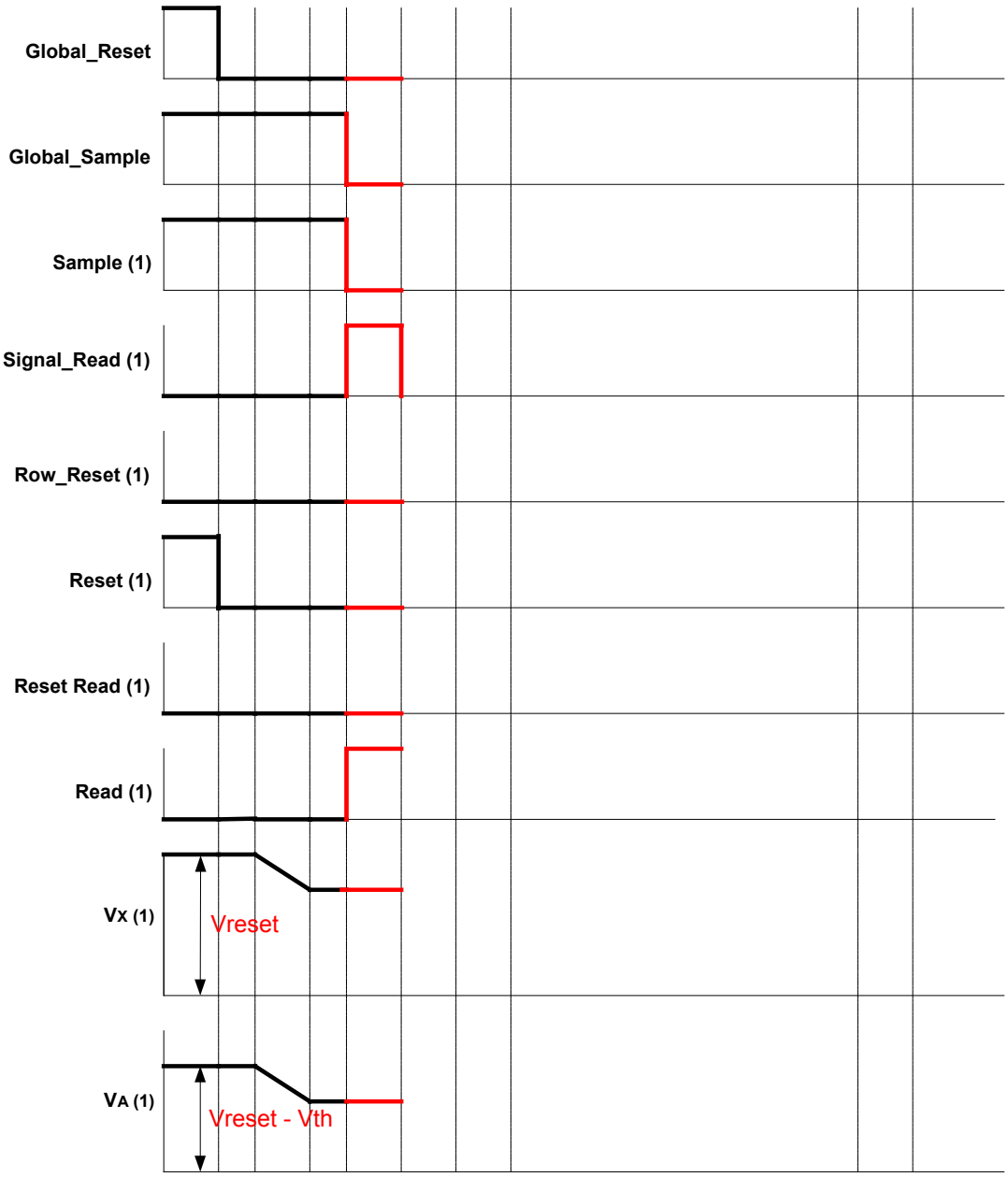

Figure 10. Sequence 5

After the trigger from Level 1 signal or the sampling period is over, row-by-row Signal_Read goes high. The voltage at Va will be read out through the output line and send down to the column. Once the sampling is closed the detector is blind to any collisions that may occur and pipelining would eliminate this dead-time.

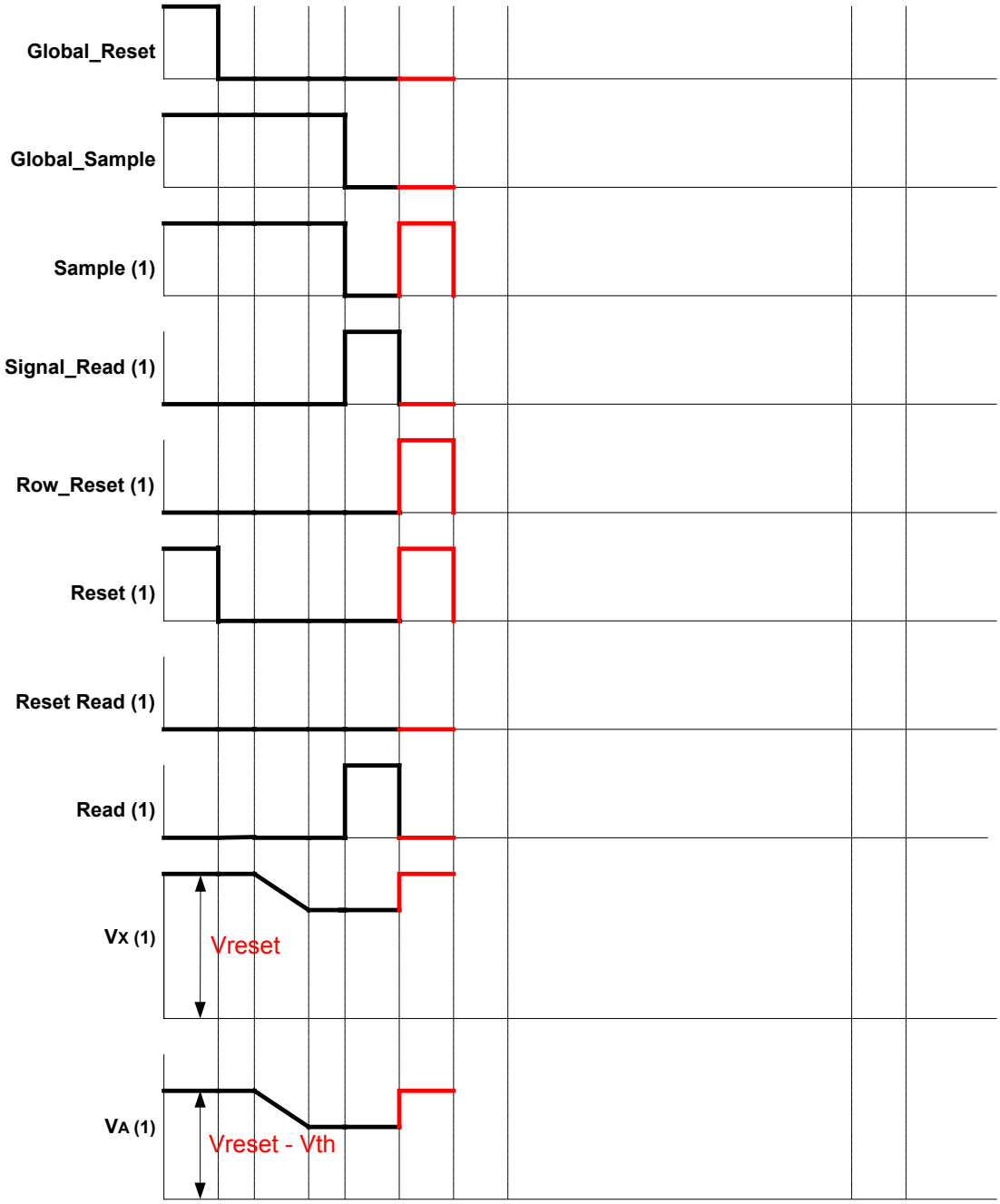

Figure 11. Sequence 6

Signal_Read goes low and Row_Reset goes high will stop the access to Va of a pixel at a particular row and will charge the Vx back up to Vreset.

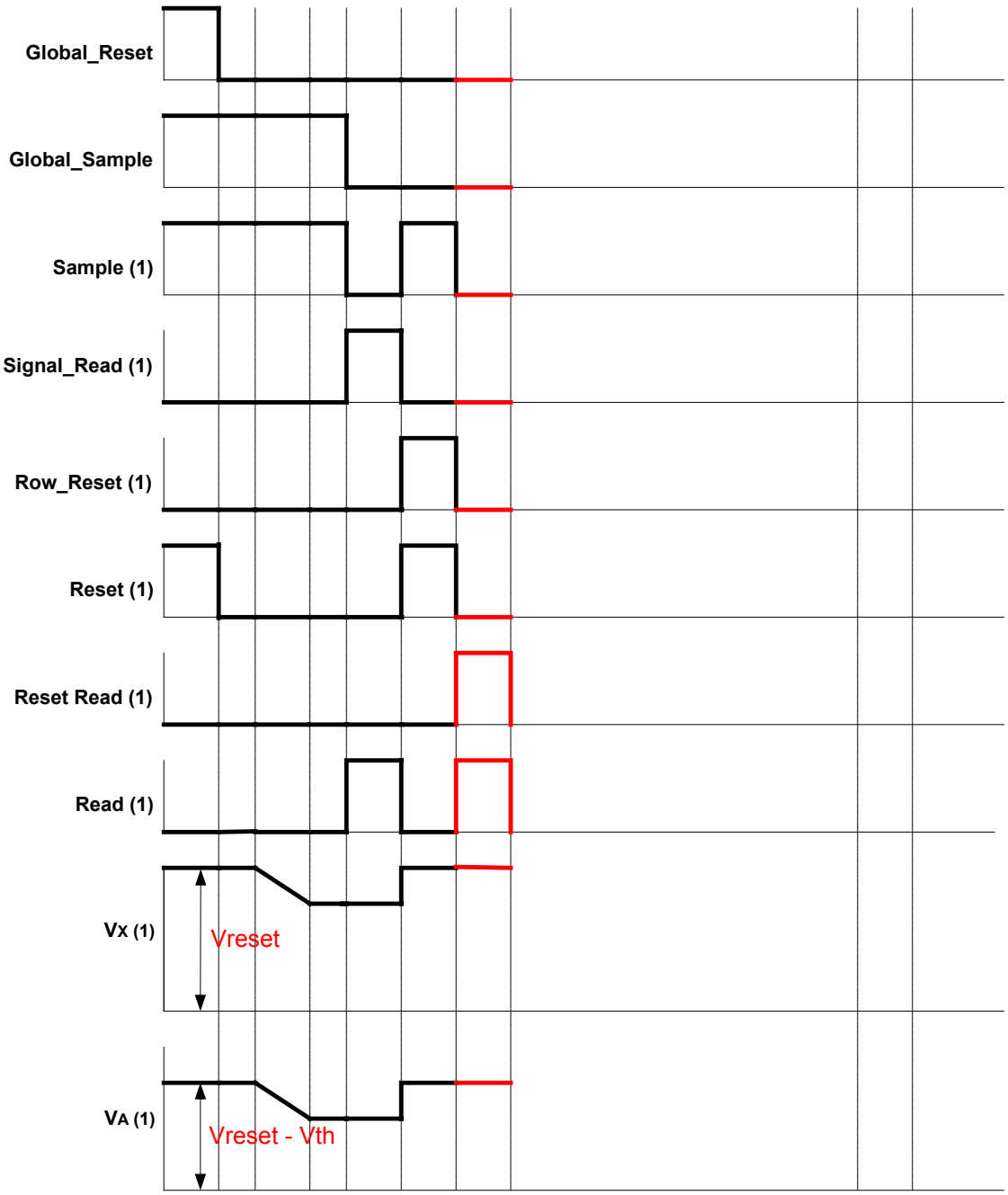

Figure 12. Sequence 7

Row_Reset goes low and Reset_Read goes high will send the Vreset out to the output line. The voltage seen at the output line is Va (Vreset-Vth). With this we can eliminates the 0^{th} order of Vth depending because we will subtract out the Vth of each pixel.

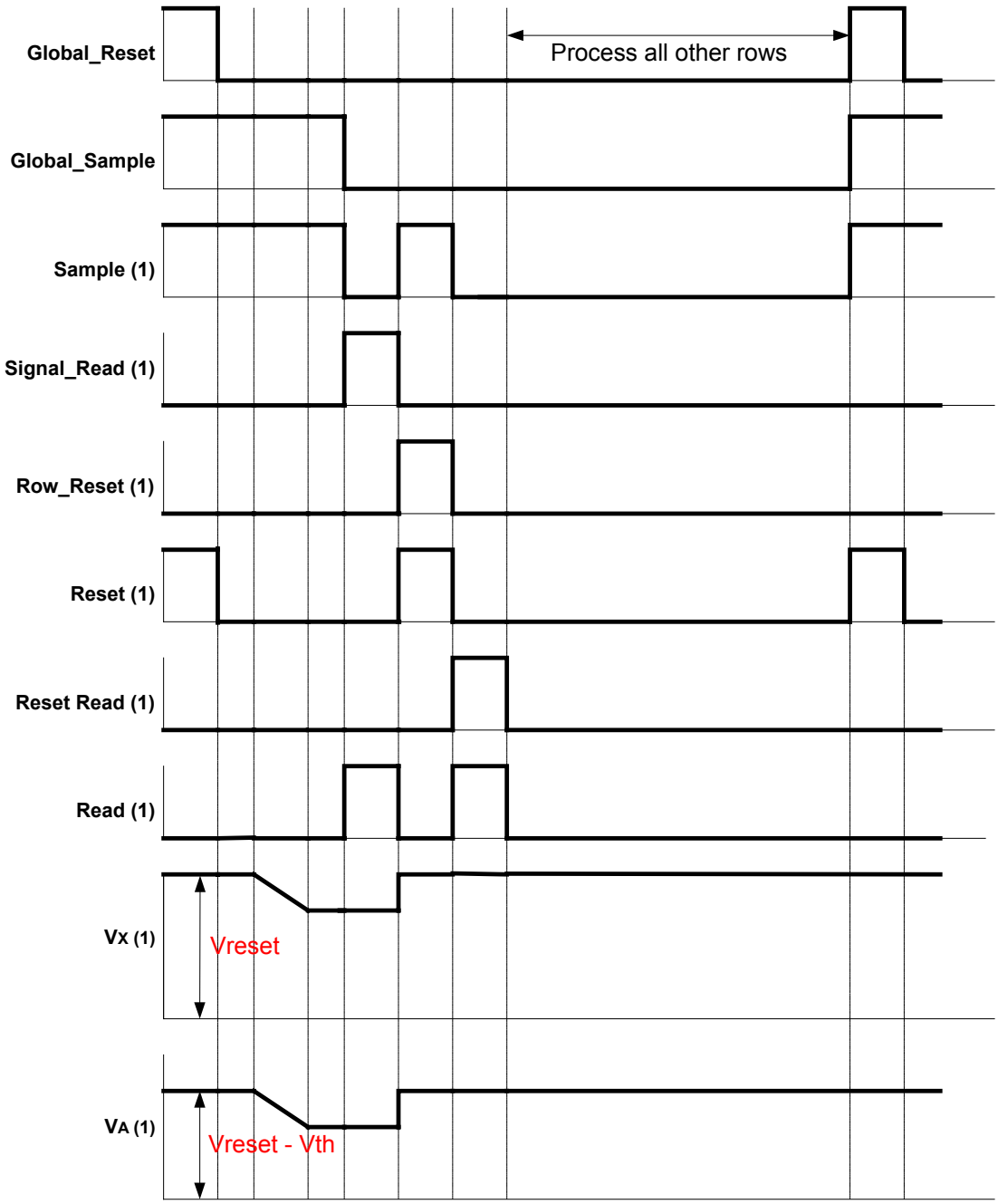

Figure 13. The whole timing diagram for one row

Figure 10 shows the whole timing diagram for a particular row. Once an operation is done on a particular row. Sequence 5 to 7 will be applied to the next row and will stop at the last row. Sequence 1 to 5 will be repeated after the last row is done.

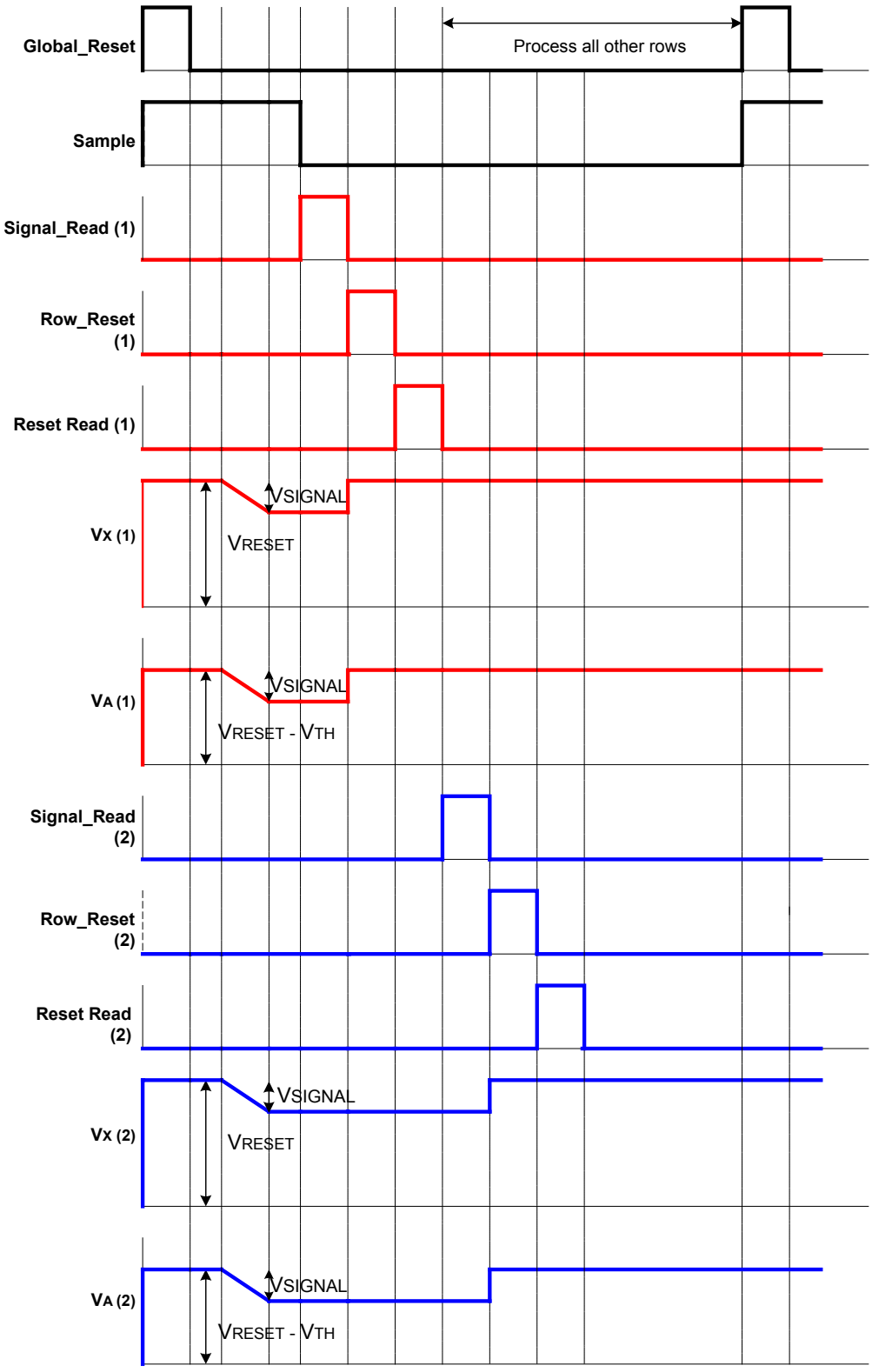

Figure 14. Timing diagram for two consecutive rows

All of the figures above are basically the sequence for the pixel to work. The Read-Read Again method is defined as how we read the signal from pixel and then we read the reset voltage from the same particular pixel.

4.2. Advantage and Disadvantages

The main advantage of the Read-Read Again method is the ability to subtract the reset noise and avoid the threshold variation of the pixel across the pixel. The actual signal excited by the particles is the difference between the reset voltage and the signal voltage. By subtracting these two signals, we are hoping that the same system noise distortion will be cancelled out.

The main disadvantage of the Read-Read Again method is time. By reading the same pixel time twice, we are basically double the access time of one pixel and extra circuitry to do this signal subtraction is required.

4.3. Possible Problems

There are couple possible issues with this Read-Read Again method. The first possible issue is the pixel has to hold the signal charge for a long time while the other rows are accessed. How well the pixel is going to hold those charges or how long it takes to acquire all of the data will be critical.

Low leakage current for the holding transistor is required. Otherwise the pixel down in the row is going to lose the data due to this leakage current. Even though we can achieve the low leakage current the time to acquire all of the data is very important. We have to make sure the time required to send out of the data will be smaller or comparable with other detectors on RHIC.

The other problem is how to integrate the pixel with the Level 1 trigger. The plan is to use the level 1 trigger to stop the sampling. What will happen if another level 1 trigger coming in when we are still acquiring the data from the pixels? One solution that coming to our mind right now is to have a couple deep analog FIFO on each pixel. Having a FIFO inside the pixel to hold the analog charges will raise the same concern about the leakage current (how well we can hold those analog voltages inside the FIFO) and how to employ the Read-Read Again method with pipelining.

4.4. Threshold voltage variation on the same pixel

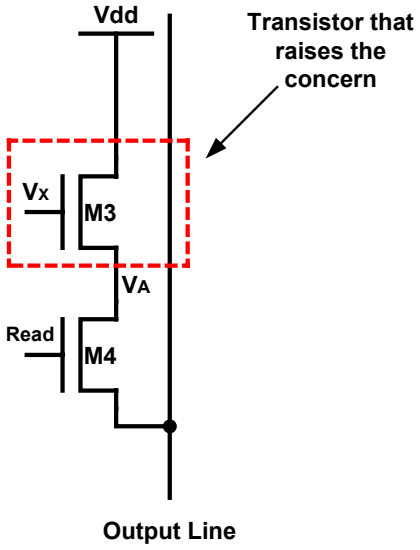

Figure 15. The source follower inside the pixel structure

The threshold voltage variation of transistor M3 itself is found to cause some concerns that we discussed below. By design the Read-Read Again method is capable of eliminating the fixed pattern noise from pixel array assuming the transistor M3 inside the pixel has a linear relationship between Vx and Va. To ensure this we will modify some details of the pixel.

The configuration of figure 15 is mostly known as source follower with a common bias current for all of the pixels on the same column. In order to understand how the source follower works, the equivalent circuit is going to be analyzed. Basic source follower is basically a transistor in series with a resistor. The gate of the transistor is where the terminal where the input voltage is applied. The resistor is connected from the source of the transistor to the ground. The output node is the source terminal of the transistor.

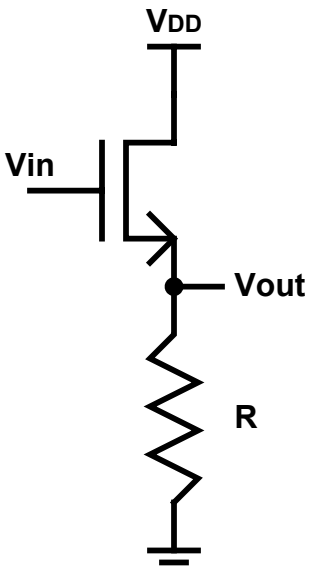

Figure 16. The basic configuration of source follower

$$V_{ds} \geq V_{gs} - V_{TH}$$
$$Vdd - Vout \geq Vin - Vout - V_{TH}$$
$$Vdd \geq Vin - V_{TH} \quad \text{.....(1)}$$

Equation (1) is the requirement for the transistor to operate in the saturation region. The current flowing through the transistor that operates in saturation region can be defined as:

$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} \left(V_{gs} - V_{TH} \right)^2$$
$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} \left(Vin - Vout - V_{TH} \right)^2 \quad \text{.....(2)}$$

Vout is also a function of the current flowing through the transistor. The relation between the Vout and current can be defined as:

$$Vout = I_D * R \quad \text{.....(3)}$$

From equation (1), (2) and (3), we can clearly see that Vout can goes up to as high as Vdd-Vth. Once Vout is equal to Vdd-Vth the current will stop flowing the transistor. This will give us the limit of how large the voltage we can apply on Vin. The maximum Vin is limited by Vdd-Vth. This means the Vreset has to be equal or smaller than Vdd-Vth.

From equation (2), we can conclude that the drain current/current flowing through the transistor is heavily depends on the input dc voltage (Vin). If Vin changes from 1.5V to 2V, Id may increase by factor of and Vgs-Vth by $\sqrt{2}$. This will introduce a substantial non-linearity in the input-output characteristic.

To alleviate the dependency of the drain current to the input voltage, the resistor can be replaced by a current source. There is no way of having an ideal current source but we can use implement it as another NMOS transistor to operate in the saturation region.

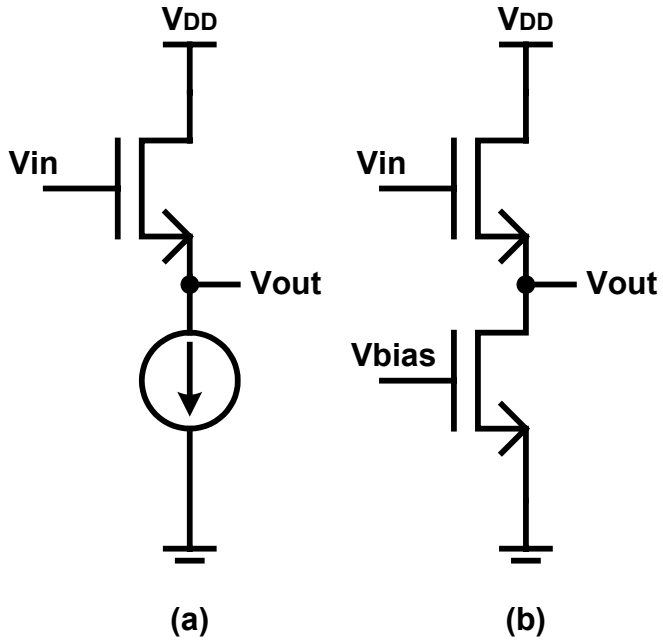

Figure 17. Source Follower using an NMOS transistor operating in the saturation region

Figure 17(a) is the source follower with the ideal current source. We will discuss figure 17(b) because it would be the actual implementation on the circuit. Even if a source follower is biased by an ideal current source, its input-output relationship will show some non-linearity due to the dependence of Vth upon the source potential. For this reason, typical source followers suffer from several percent of non-linearity between the input and output[5].

The simulation outputs are shown in figure 16 and figure 17(b) where it is demonstrated that there is no linear relationship between the input and output.

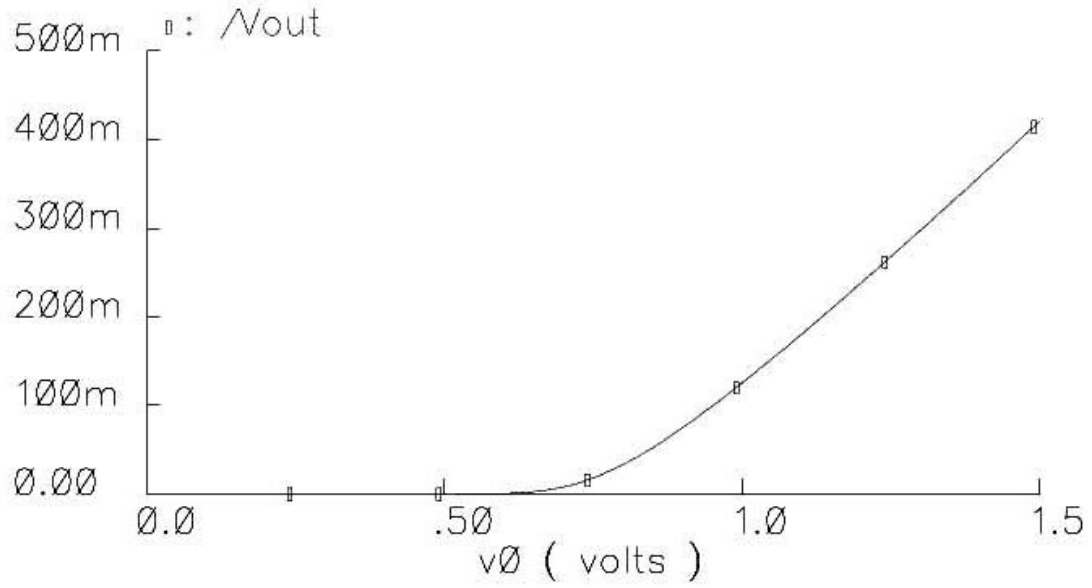

Figure 18. Input vs Output voltage for figure 16

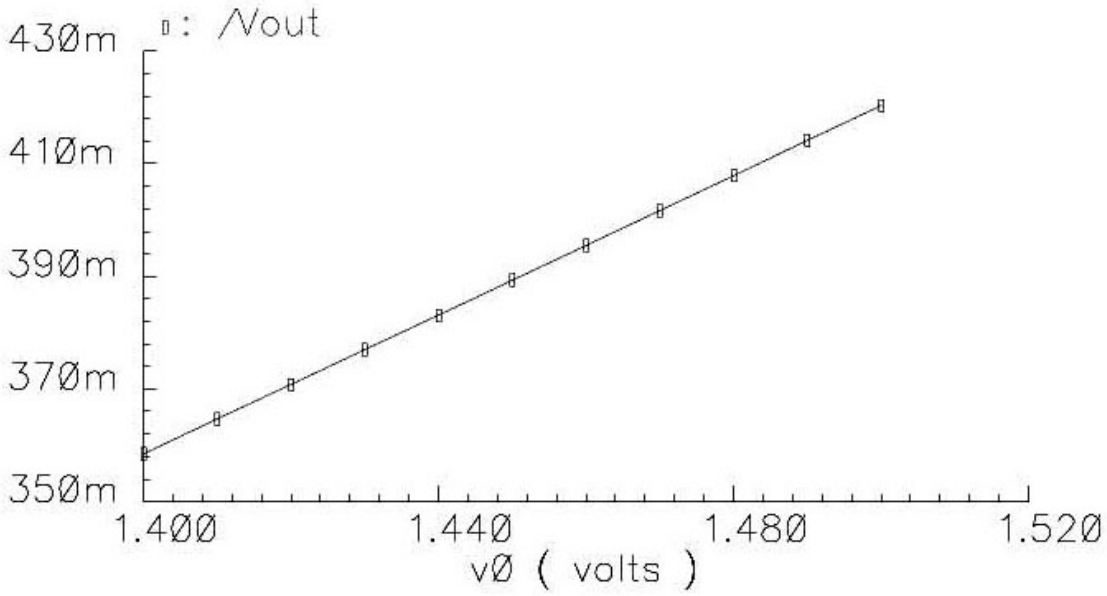

Figure 19. Zoom in of figure 18

To show the non-linearity relationship between the input and output voltage, we measure the output voltages when then inputs are 1.4V and 1.5V.

$$Vin = 1.4V \rightarrow Vout = 358.545mV$$
$$Vdrop_{1.4V} = 1.04146V$$
$$Vin = 1.5V \rightarrow Vout = 420.34mV$$
$$Vdrop_{1.5V} = 1.07966V$$
$$\triangle Vdrop = 38.205mV = 3.66\%$$

The next figure is the zoom in plot of the input vs output voltage for figure 17(b).

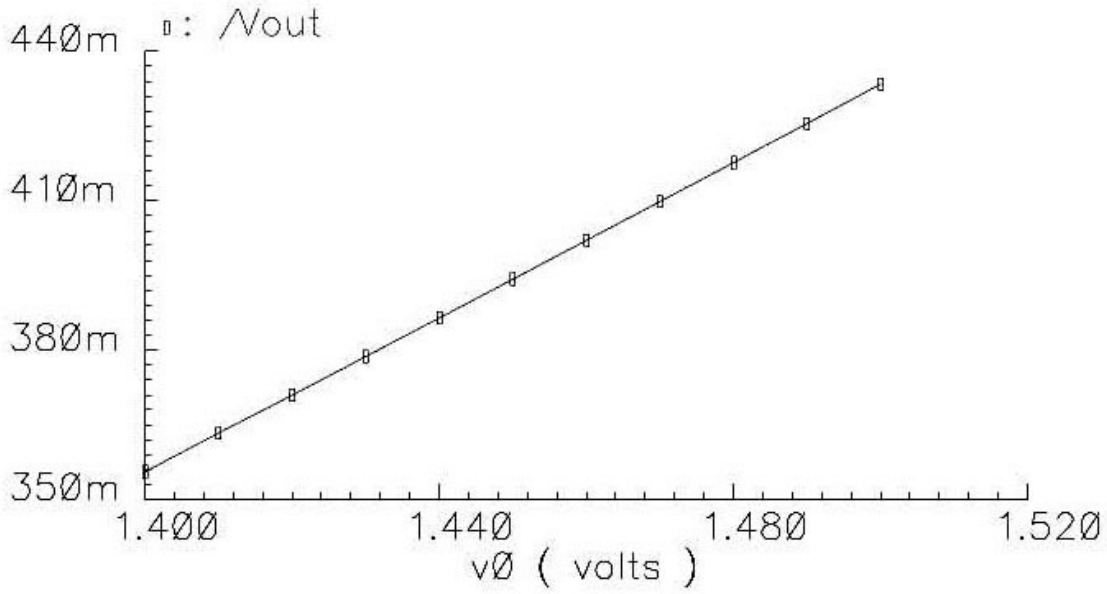

Figure 20. Input vs Output voltage plot for figure 17(b)

$$Vin = 1.4V \rightarrow Vout = 355.682mV$$
$$Vdrop_{1.4V} = 1.04432V$$
$$Vin = 1.5V \rightarrow Vout = 433.354mV$$
$$Vdrop_{1.5V} = 1.06665V$$
$$\triangle Vdrop = 22.328mV = 2.13\%$$

From the above calculations, we can see that having a current source on each pixel improves the non-linearity relationship between the input and output voltage. However there is still a problem due to variation of the threshold voltage of each pixel depending on the input voltage.

In order to understand, why the threshold voltage of a transistor varies. The formula to calculate the threshold voltage is:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

We can clearly see the non-linearity is due to the body effect (V_{SB}). In order to eliminate the body effect, we can tie the substrate to the source.

This approach is only possible for p-type transistor because all of the n-type transistors usually share the same substrate in regular CMOS process using the wafer as the p-substrate. Having the epi-layer on top of the wafer gives us the advantage of the possibility of using n-type transistor and still able to eliminate the body effect toward the threshold voltage.

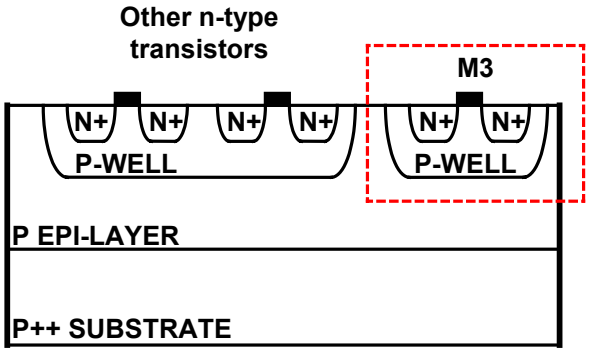

Figure 21. Partial Cross section of one pixel

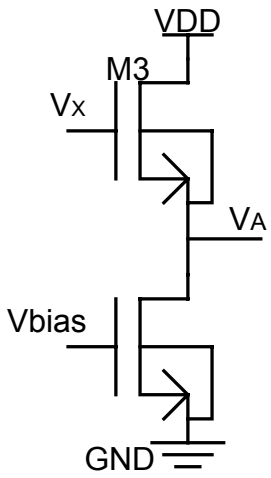

Figure 22. Source follower with substrate connected to the source

Table 1 will show how the source follower on figure 19 compare to the one on figure 17(b). The only different between these two source followers is how the substrate on the input transistor is connected. The substrate of the structure on figure 17(b) is hooked up to a ground (all n-type transistors are sharing the same substrate) and the substrate of the input transistor in figure 19 is connected to the source of the transistor (having a separate well for the substrate).

Table 1. Threshold voltage variations comparison

Substrate tied up to	VDD	Vx	Va	Vdrop	Diff	Percent (%)
Ground	3.3	1.7	0.4065	1.2935	0.0242	1.8746
		1.8	0.4822	1.3178		
Ground	5	2.4	0.9563	1.4437	0.0196	1.3547
		2.5	1.0368	1.4632		
Source	3.3	1.7	0.5282	1.1718	0.0027	0.2330
		1.8	0.6255	1.1745		
Source	5	2.4	1.2190	1.1810	0.0011	0.0965
		2.5	1.3178	1.1822		

From table 1, we can clearly see that the structure on figure 19 (bottom two rows of Table 1) works a lot better than the one on figure 17(b). The threshold voltage is varying well below 1% range and the Read-Read Again method can be applied with this structure. Implementing the source follower from figure 19 to our current pixel structure can be done by adding one more n-type transistor for the bias current and the substrate of the input transistor of the source follower is connected to the source. The new proposed pixel cell structure can be seen below.

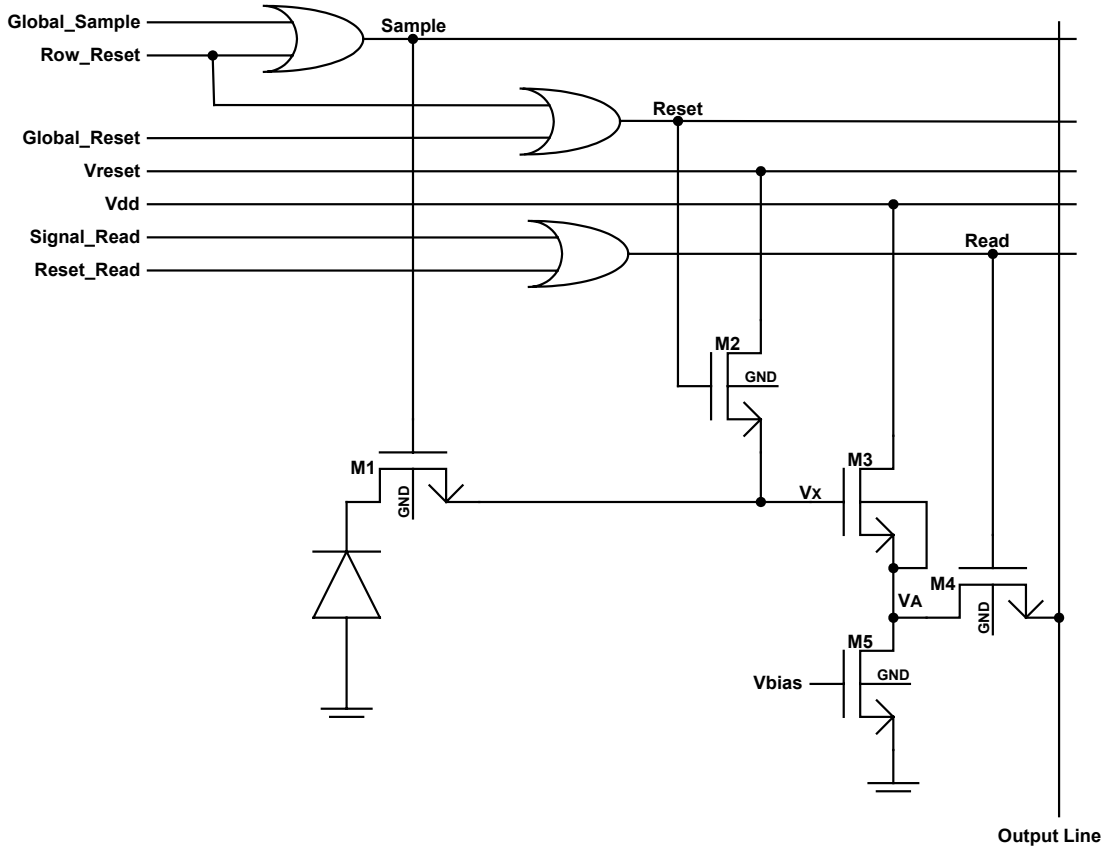

Figure 23. New Proposed Pixel Structure

5. Amplifying the signal

The signal sent down each column will be amplified before it is being digitized. The amplifier will serve as the gain circuit and also the subtraction circuit. The circuit can be seen on figure 24[6].

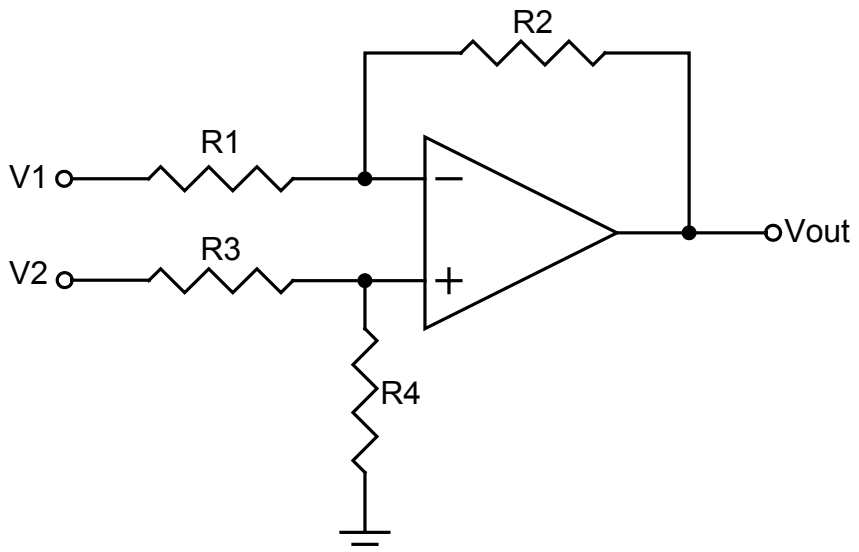

Figure 24. Difference Amplifier

We will use the configuration from figure 24 to do the subtraction and gain function. We will try to analyze figure 24 so we can clearly see how it will perform those two functions. There are many ways to analyze this type of structure but the easiest one is probably using superposition because this is a linear network.

Doing superposition, we will first reduce V2 to zero, which can be done by grounding the terminal to which V2 is applied and then find the corresponding output voltage that is entirely due to V1.

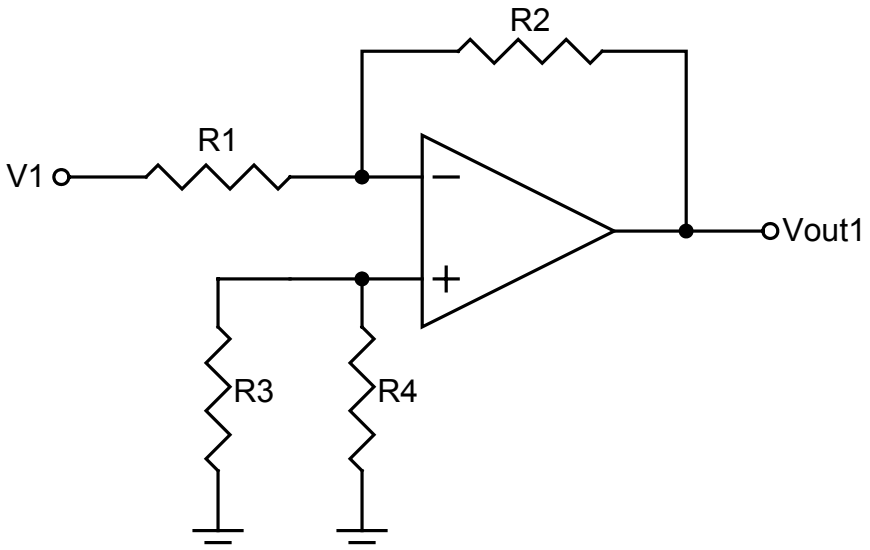

Figure 25. Superposition with only V1 input

The output due entirely to V1 will be called Vout1. The transfer function of this configuration has no effect from R3 and R4 because there are no current flows through either of them. The relation between the input voltage with the output voltage can be expressed as the following:

$$Vout1 = -\frac{R2}{R1}V1$$

Next, we will reduce V1 to zero and evaluate the corresponding output voltage that is due entirely to only V2 input voltage. This configuration is knows as the non-inverting configuration with and additional voltage divider connected to the input terminal.

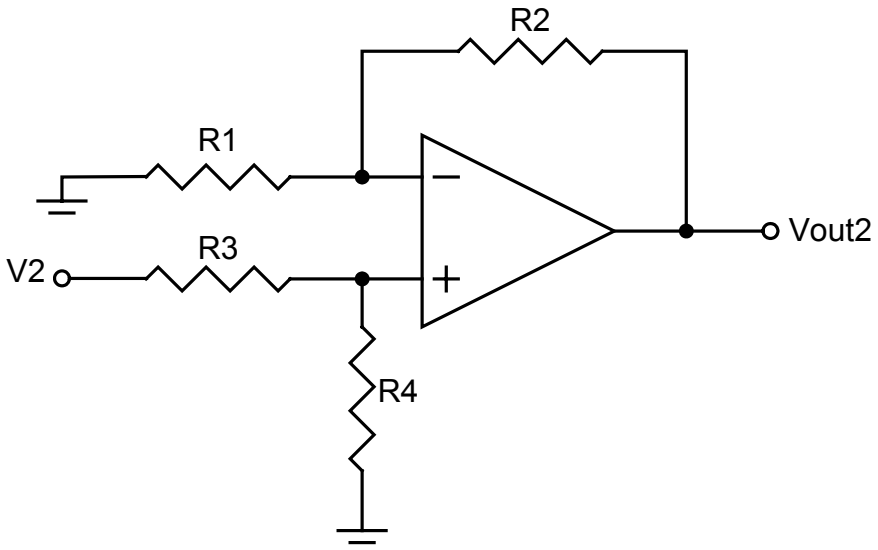

Figure 26. Superposition with only V2 input

The output voltage can be expressed as:

$$Vout2 = V2\frac{R4}{R3+R4}\left(1+\frac{R2}{R1}\right)$$

The superposition approach tells us that the output voltage is basically the same with the sum of Vout1 and Vout2. Therefore the Vout = Vout1+Vout2, Vout can also be written as follow:

$$Vout = -\frac{R2}{R1}V1 + \frac{1+R2/R1}{1+R3/R4}V2$$

The Vout expression does not clearly show how the subtraction and the gain functions will be performed. By setting $R2/R1 = R4/R3$, we can rewrite the expression of Vout to be:

$$Vout = \frac{R2}{R1}(V2 - V1)$$

(V2-V1) term shows how the subtraction function will be performed and the R2/R1 will be the term to determine the gain of the amplifier.

The first signal (Signal_Read) will hold in V1 and then we are going to read the second signal (Reset_Reset) and hold in V2. With this approach we can have only one output line for each column.

A two-stage architecture for the operational amplifier will be used and the opamp has to be able to work with 50MHz input frequency.

6. Digitizing the signal

An Analog-to-Digital Converter is used to digitize the amplified signal. The ADC is currently a 3-bit ADC. It is a latched comparator ADC so the power consumption is pretty low [7]. Low power is important because we will have one ADC on each column. We can set a threshold at the reference low of the ADC so we have the flexibility to choose a lower threshold for the signal to be digitized. This is useful to reduce or eliminate non-useful information to be sent out.

This type of comparator operates simply with only one-phase clock. The comparator is consists of a power switch transistor, input transistors and current cutting transistors with feedback inverters. This comparator can be seen on figure 27.

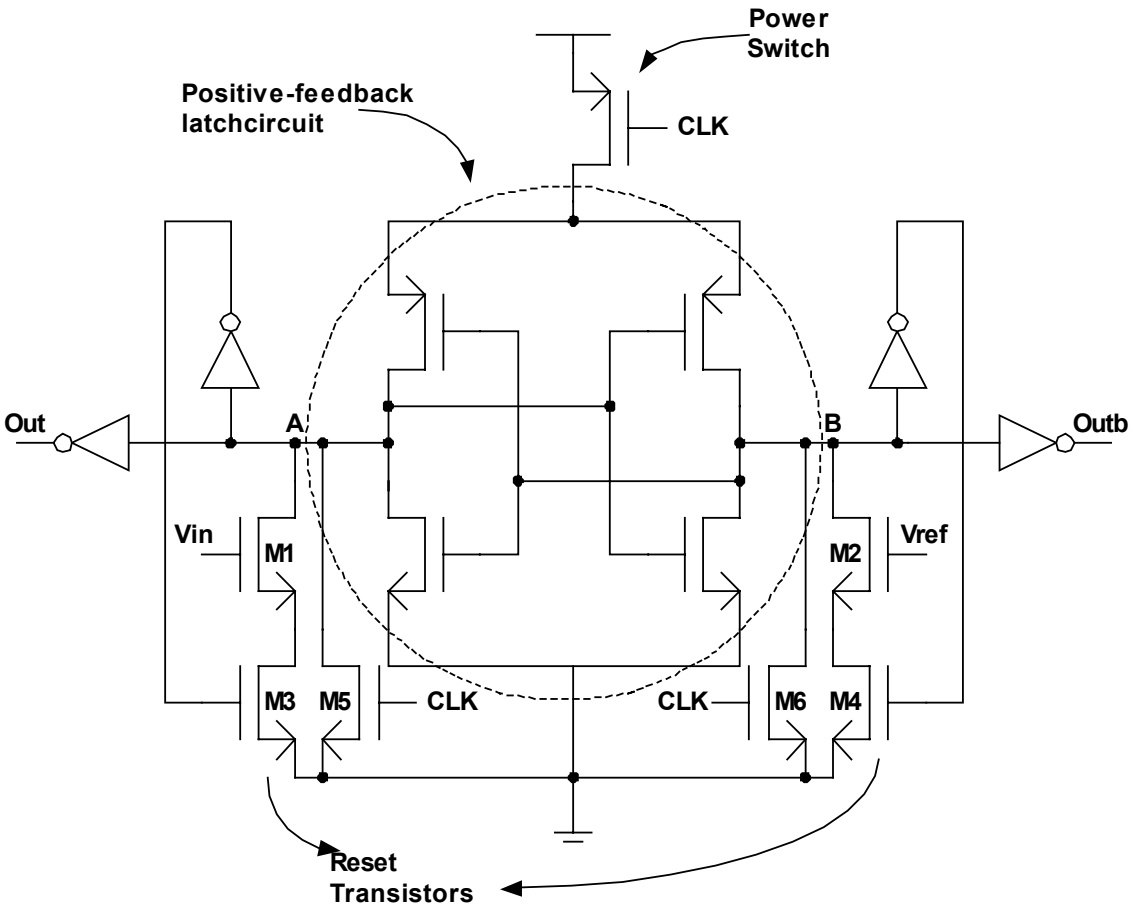

Figure 27. Transconductance latched comparator

This comparator performs different functions depends on the clock phase. When the clock signal is high, the comparator is in the reset mode, and when it is low, it is in the

compare mode. A timing diagram will show on the next figure to clearly show these two different phases of the comparator.

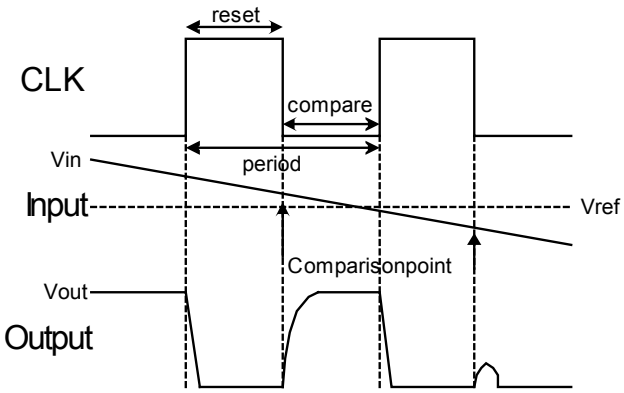

Figure 28. Timing diagram of the comparator

More details about how this comparator works will be discussed. In the reset phase, the power switch is off; M5 and M6 are on. This will cause node A and B pre-charge to the ground level. Input transistors M1 and M2 are on because $V_{GS} \rangle V_{TH}$. And the difference between these transistors will remain unchanged even if no current flows through them.

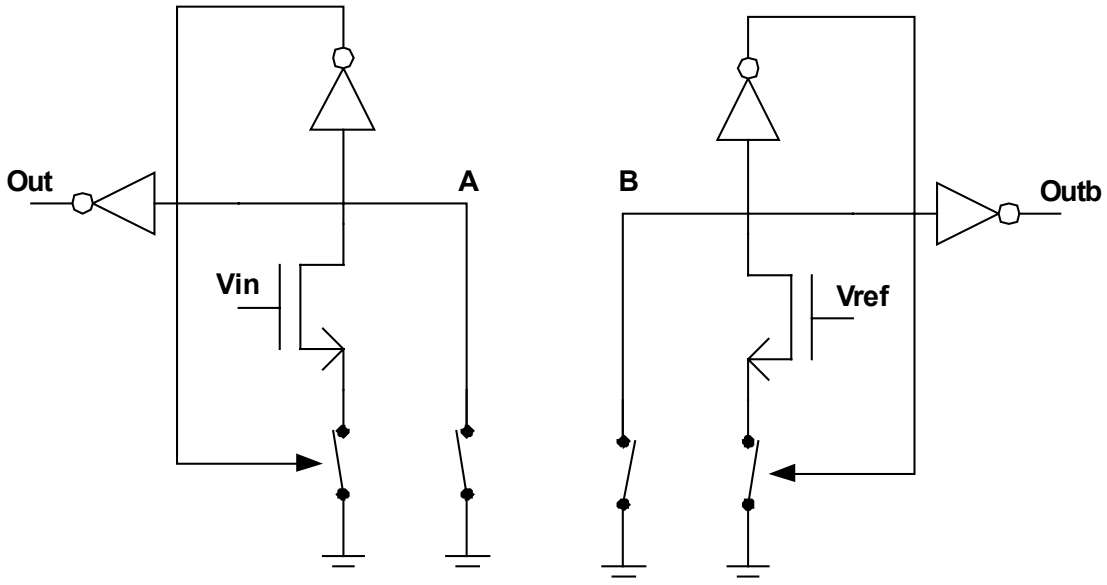

Figure 29. Reset Phase

The second phase is the compare phase; this is the phase where the comparator will decide whether the input voltage is bigger or smaller than the reference voltage. In this phase, power transistor is on. At the beginning of this phase, the reset transistors (M5 and M6) are off. Therefore, the voltage different comes between node A and B is due to the difference in the transconductance of the input transistors and the positive-feedback latch circuit amplifies it to the full range. When the voltage at either node A or B reaches the voltage level of Vdd, M3 or M4 will be off and cut the current off.

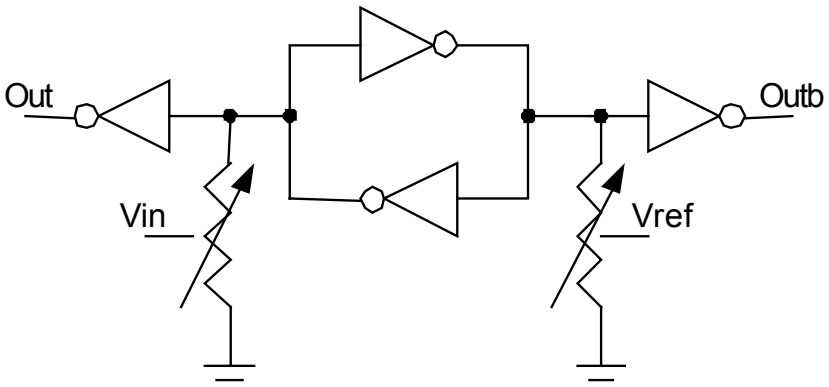

Figure 30. Compare Phase

It is difficult to compare voltages if both are below the threshold voltage of the input transistors. A complementary structure circuit is used for low reference voltage. Instead of using n-type transistor, p-type transistor is used as the input transistor. The lower half of the comparators will use the p-type input transistors and the upper half of the comparators will use the n-type input transistors.

This approach of comparator has couple advantages compare to others architecture. Some of the advantages are[7]:

- Low input capacitance
- Low kick-back noise
- Low power consumption
- High speed
- Can compare the voltage over VDD

Our ADC is designed to work with 50MHz clock and 3-bit resolution. Increasing the resolution of our ADC to 5-bit is possible if it is required in the future.

7. Conclusion

Monolithic active pixel detector fabricated in regular CMOS technology has been proven to be achievable by IreS/Lepsi work [1]. The goal of having the detecting pixel and the readout electronics integrated onto the same low-resistivity silicon wafer is also feasible.

The idea of Read-Read Again method seems to be pretty reasonable but it has not been actually proven. The concept seems to be able to get rid of the systematic noise but the system will still suffer from the random noise.

The Read-Read Again method will require longer read-out time compare to a conventional read-out. The goal of this study is trying to make the read-out time per pixel to be around 130nS. This means for 50 pixels per column array it will take about 6.5 uS.

The threshold voltage variation seems to the biggest challenge for this concept to work. More research needs to be done in order to reduce this threshold voltage variation. The most important part is to get more information about the diode. The actual diode behavior will pretty much determine whether this Read-Read Again concept is doable.

8. Bibliography

[1] G. Deptuch, "CMOS Pixels for Particle Tracking," *IEEE NPSS Silicon Pixel/CCD Tracking Detectors Course*, July 10-11 2001, Colorado, USA, 2001.

[2] Fill Factory, "High Fill Factor N-Well Pixel," *http://www.fillfactory.com/htm/technology/htm/high_fill.htm*, April 1, 2002.

[3] G. Deptuch, "Monolithic Active Pixel Sensors for Charged Particle Tracking," *Brookhaven National Laboratory RHIC R&D Workshop*, November 2001.

[4] B. Dierickx, G. Meynants, D. Scheffer, "Near-100% fill factor standard CMOS active pixel," *IEEE CCD & AIS Workshop*, Brugge, Belgium, June 5-7, 1997, Proceedings p.P1

[5] B. Razavi, "Design of Analog CMOS Integrated Circuits," New York, McGraw-Hill, 2001.

[6] A. Sedra, K. Smith, "Microelectronic Circuits," New York, Oxford University Press, 1998.

[7] J. Terada, Y. Matsuya, F. Morisawa, Y. Kado, "8-mW, 1-V, 100MSPS, 6-BIT A/D Converter Using a Transconductance Latched Comparator," *The 2nd IEEE Asia Pacific Conference on ASICs*, Aug 28-30, 2000.